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QUARTERLY TECHNICAL REPORT #2
(7/1/92 - 9/30/92)

Sponsored by:
Defense Advanced Research Projects Agency
Defense Sciences Office (DSO)
Vacuum Microelectronics Program
ARPA Order No. 8162/07 & /09 Program Code No. 2G10
Issued by DARPA/CMO under Contract # MDA972-92-C-0034

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Title of Work:

RF VACUUM MICROELECTRONICS

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1.0 Emitter Fabrication

1.1 Mask Design and Procurement

1.1.1 Mask Set #1

Most of mask set #1 was delivered in the previous quarter. In the second quarter (July) we took delivery of the final mask layer and re-ordered one other layer due to problems that we discovered with the original design rules. All of the mask layers were checked for registration and found to be within acceptable limits. We found that all the tip sizes were easily resolved with our standard lithographic techniques. Even 1μm diameter opening to etch the smallest molds were easily obtained. The key problem that we encountered in using the newly designed mask was poor layer to layer registration of patterns defined prior to plating (on the silicon mold) to patterns defined after plating on the silver substrates. It appears that the dimensional stability of the silver is not as good as a typical semiconductor. As a result, there was about 10μm of runout per centimeter when we aligned the gate metal pattern to the tip arrays. This amount of runout is tolerable but unexpected and did result in the loss of some samples due to subsequent emitter to gate shorting. Note that the tips themselves are made with a self-aligned technique and do not require any layer to layer registration; tip geometry was not affected by the problems in layer registration.

We also demonstrated that we could pattern the emitter metal as well as the gate metal... a significant advantage for fabricating the low capacitance emitters necessary for high frequency operation. The emitter patterning feature was demonstrated in an off-line experiment and not incorporated into our first design of experiments.

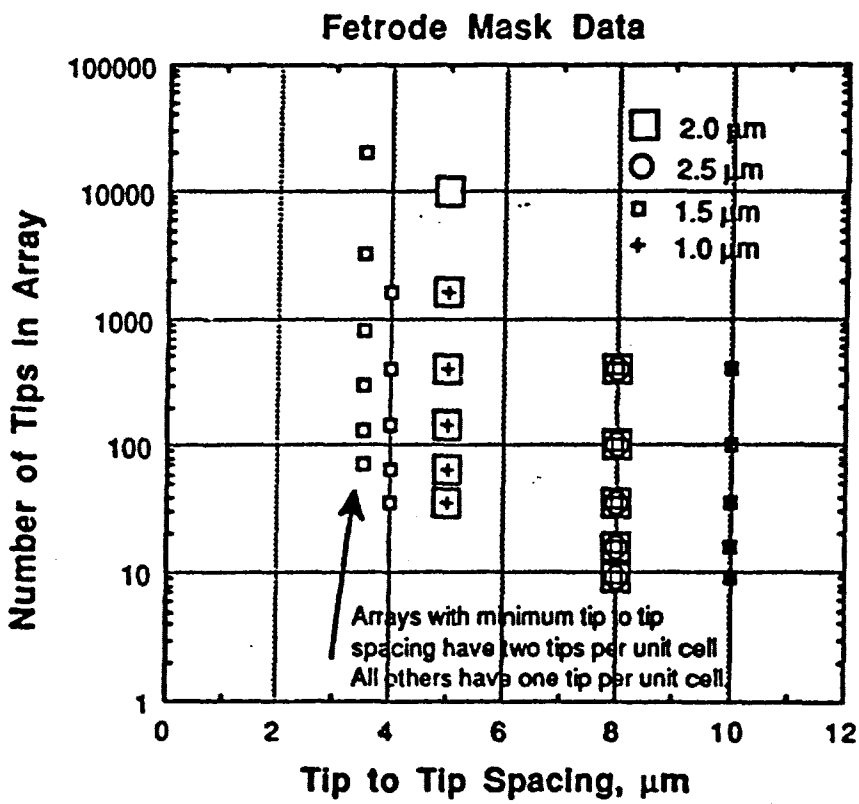

Fig. 1 - Graphic description of the size and spacing of emitter tip arrays on mask set #1.

Figure 1 is a graphical representation of the test patterns available on this mask set. Each point represents a single array with ordinate equal to the tip spacing and abcissa equal to the number of tips in the array. Based on geometry alone we expect a factor of three difference in cutoff frequency (ratio of transconductance to capacitance) and three orders of magnitude difference in current density. Material parameters will further increase the range of cutoff frequency and current density.

1.2 Process Optimization Experiments

1.2.1 Process #1.1

We designed an L16 orthogonal array to study 4 critical process parameters and a number of vacuum processing and geometrical factors. The table below summarizes the process parameters that were varied in the experiment (test parameters to be varied during testing are not listed). Each sample is about 1 inch square and contains 25 chips (unit cells), each unit cell contains more that 50 emitter arrays.

Table I - First FETRODE L16 experiment. Critical process parameters.

No.	Tip	Etch	Diel.	Thk.	Gate
1	Ta	5 min	SiN	4kÅ	1kÅ
2	Ta	7 min	SiN	4kÅ	2kÅ
3	Ta	9 min	SiO	6kÅ	1kÅ
4	Ta	11 min	SiO	6kÅ	2kÅ
5	Mo	5 min	SiN	6kÅ	2kÅ
6	Mo	7 min	SiN	6kÅ	1kÅ
7	Mo	9 min	SiO	4kÅ	2kÅ
8	Mo	11 min	SiO	4kÅ	1kÅ
9	Au	5 min	SiO	4kÅ	1kÅ
10	Au	7 min	SiO	4kÅ	2kÅ
11	Au	9 min	SiN	6kÅ	1kÅ
12	Au	11 min	SiN	6kÅ	2kÅ
13	Pt	5 min	SiO	6kÅ	2kÅ
14	Pt	7 min	SiO	6kÅ	1kÅ
15	Pt	9 min	SiN	4kÅ	2kÅ
16	Pt	11 min	SiN	4kÅ	1kÅ

Since we had not yet performed any emission tests, the only response function available to this point was the geometry of the emitter tips and gate. We studied the aperture size as a function of the process because of the importance of this parameter and the relative ease with which it can be measured in an SEM. This parameter will strongly influence the eventual turn-on voltage of the emitters. We considered the aperture size of the 2.5μm tips as a function of three process variables: Type of dielectric, dielectric thickness and gate metal thickness. We tested the hypothesis that the two levels considered for each parameter DO NOT affect the aperture opening. At a 95% confidence level this hypothesis was rejected only for the gate metal thickness. That is, we found that the aperture size WAS dependent on the gate thickness as shown in the table below.

Table II - Analysis of the effects of three process parameters on the physical structure of the emitter tips.

Process Parameter	Level	Average Aperture of 2.5μm Tips	Standard Deviation	Is Difference Statistically Significant?
Dielectric Type	SiO_2	0.87 μm	0.25 μm	No
	Si_3N_4	0.72 μm	0.15 μm	
Dielectric Thickness	4000 Å	0.81 μm	0.18 μm	No
	6000 Å	0.75 μm	0.24 μm	
Gate Metal Thickness	1000 Å	0.91 μm	0.18 μm	Yes
	2000 Å	0.65 μm	0.13 μm	

In the next quarter we will continue to study the effects of process parameters on both electrical and physical characteristics of the emitter. Other response functions that will be studied in the next quarter are breakdown voltage of the dielectric as a function of thickness, type of dielectric and tip size and leakage current between emitter and gate as a function of these same parameters. Of course, the key response functions for high frequency devices are the turn-on voltage of the array and the maximum emission current density. The effect of process variables on these two parameters will be studied in detail.

2.0 Emitter Testing

2.1 Design and Fabrication of Test Chamber

The test chamber has been completed. It is capable of testing 16 devices on 16 separate headers. Pressures in the low 10^{-9} range have been obtained after bakeout of test devices mounted on the headers. Devices are baked using quartz lamps in the vacuum chamber. A thermocouple mounted on a dummy header is used to monitor device temperature during bakeout. The anodes can be electron bombarded unitl red hot by individual filaments. This anode processing prevents outgassing of the anode during device testing as reported by Spindt.

We have begun initial testing using the Keithley SMU's described in the previous report. We verified the operation of the test chamber by reproducting IV characteristics of a number of Spindt cathodes.

3.0 Low Work Function Materials

3.1 Identify Candidate Materials

We have identified a number of candidate materials that can be used to fabricate the emitter tips with our process. The development of the plating process to create self supporting substrates has opened up the choice of materials considerably. With the current process using KOH to separate the silicon mold from the silver substrate, we can use Au, Pt and LaB_6 (all three have negligible etch rates in KOH) and any other material impervious to KOH that can be deposited at room temperature into the silicon mold. A number of other materials can be used to coat the tips prior to dielectric and gate metal deposition. We have demonstrated Mo and Ta (two of the lowest work function elements); other possibilities are metal alloys or compounds that are not attacked by dilute HF (used to remove the oxide or nitride layer from the tip). Note that coating the tips after the mold is removed causes some loss of tip sharpness (the tip radius is of the order of the metal coating). Finally, because of the structure of the final emitter tip and

gate, we can coat the device *in-situ* from a directional source; the gate aperture acts as a shadow mask to prevent the coating from shorting the gate and emitter.

4.0 FEA Equivalent Model

A preliminary equivalent circuit model for the FEA has been generated. It is primarily based on calculation of capacitance and is applicable only for small signal operation with the anode to emitter voltage larger than the gate to emitter voltage. Capacitance calculations that neglect fringing fields at the edges of the gate metal or near the emitter tips have been made for the arrays on mask set #1. Considering only the largests arrays, those of 400 tips or more, capacitance per tip ranges from a low of 0.9 fF/tip for a 20,000 tip array with 3.5μm tip spacing and a 6000 Å SiO_2 dielectric to a high of 20 fF/tip for a 400 tip array with 10μm spacing and a 4000 Å Si_3N_4 dielectric. Measurement verification of these capacitances will follow in the next report. The transconductance must be obtained from measured IV characteristics and is therefore unknown. The gm will have the form:

$$g_m \equiv \frac{\partial I_e}{\partial V_g} = \frac{2\beta I_o}{V_g^3} e^{\left(\frac{-\beta}{V_g^2}\right)} = \frac{2\beta I_e}{V_g^3}$$

Where Ie is the emitter current and Vg is the gate voltage, beta is a constant dependent on tip geometry and work function and Io is a constant proportional to the number of tips. The function is clearly very sensitive to the operating point. Capacitance reduction will play only a small role in maximizing cutoff frequency, the main effect will come from maximizing the current density per tip and lowering the emission potential.